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NMOS

MPS
6525
TRI-PORT
INTERFACE

6525 TRI-PORT INTERFACE

CONCEPT . . .

The 6525 TRI-PORT Interface (TPI) is designed to simplify the Implementation of complex I/O operations in microcomputer systems. It combines two dedicated 8-bit I/O ports with a third 8-bit port programmable for either normal I/O operation or priority interrupt/handshaking control. Depending on the mode selected, the 6525 can provide 24 individually programmable I/O lines or 16 I/O lines, 2 handshake lines and 5 priority interrupt inputs.

FEATURES:
- 24 individually programmable I/O lines or 16 I/O lines, 2 handshake lines and 5 interrupt inputs.
- Priority or non-priority interrupts
- Automatic handshaking
- Completely static operation
- Two TTL Drive Capability
- 8 directly addressable registers
- 1 MHz, 2MHz and 3MHz operation

6525 REGISTERS

*000	R0	PRA – Port Register A
001	R1	PRB – Port Register B
010	R2	PRC – Port Register C
011	R3	DDRA – Data Direction Register A
100	R4	DDRB – Data Direction Register B
101	R5	DDRC – Data Direction Register C
110	R6	CR – Control Register
111	R7	AIR – Active Interrupt Register

*NOTE: RS2, RS1, RS0 respectively

ORDER NUMBER:

MXS 6525 __

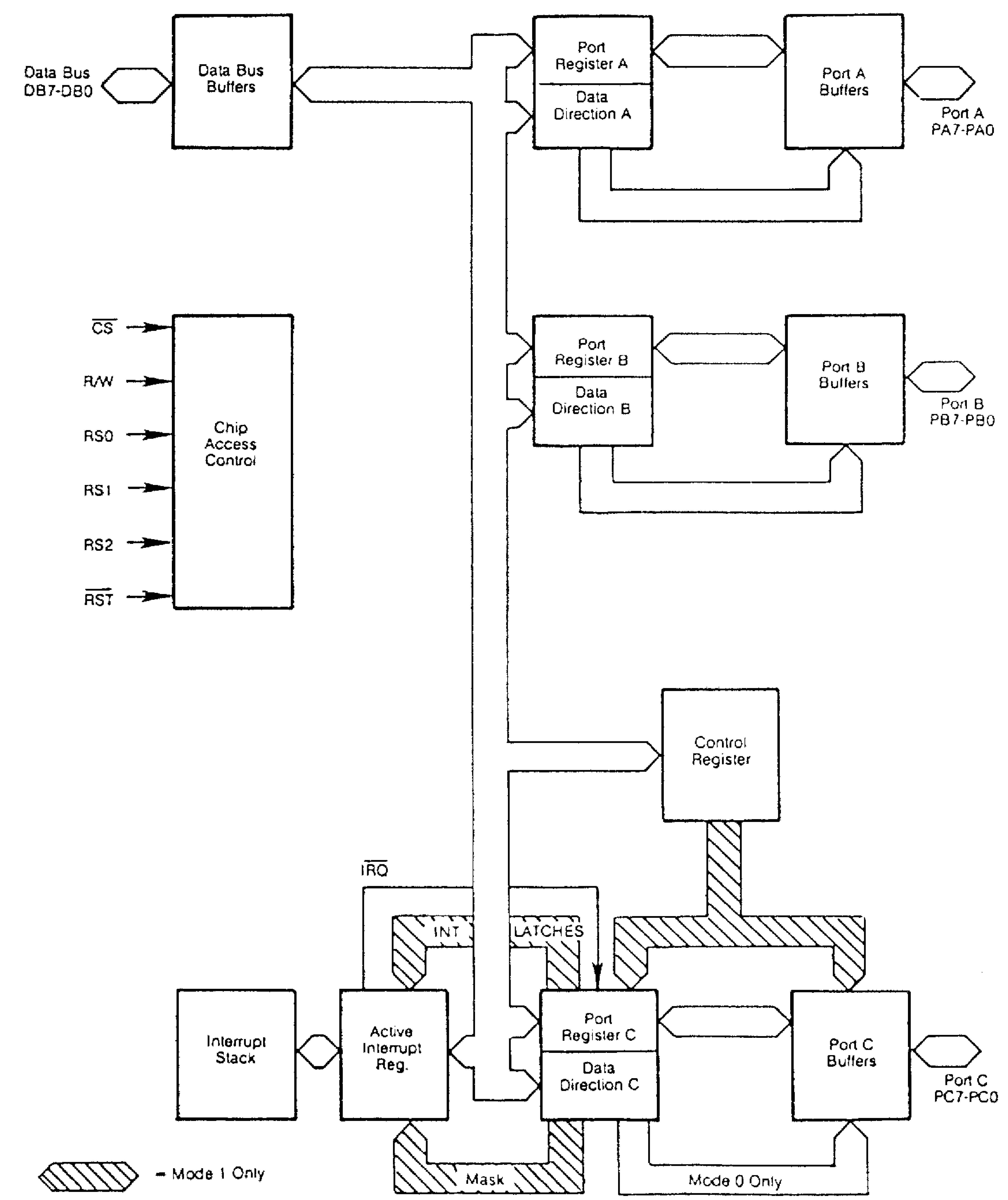
SPEED RANGE
NO SUFFIX = 450 ns
A = 225 ns
B = 155 ns

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

6525 PIN CONFIGURATION

V_{SS}	1	40	DB7
PA0	2	39	DB6
PA1	3	38	DB5
PA2	4	37	DB4
PA3	5	36	DB3
PA4	6	35	DB2
PA5	7	34	DB1
PA6	8	33	DB0
PA7	9	32	PC7
PB0	10	31	PC6
PB1	11	30	PC5
PB2	12	29	PC4
PB3	13	28	PC3
PB4	14	27	PC2
PB5	15	26	PC1
PB6	16	25	PC0
PB7	17	24	RS0
$\overline{CS}$	18	23	RS1
R/W	19	22	RS2
V_{DD}	20	21	$\overline{RES}$

6525 INTERNAL ARCHITECTURE



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MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

COMMENT

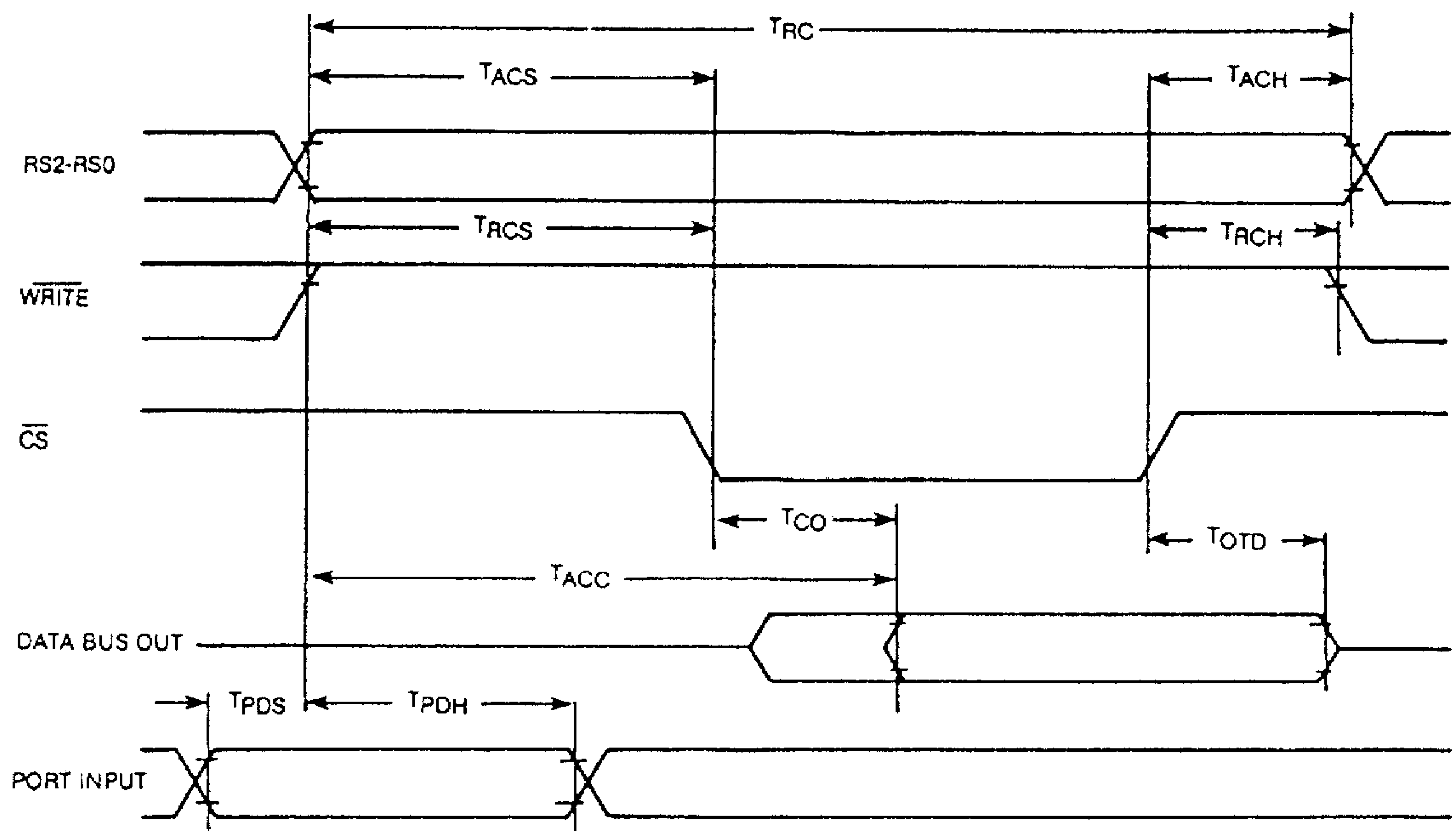
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0V, T_A = 0° to 70°C)

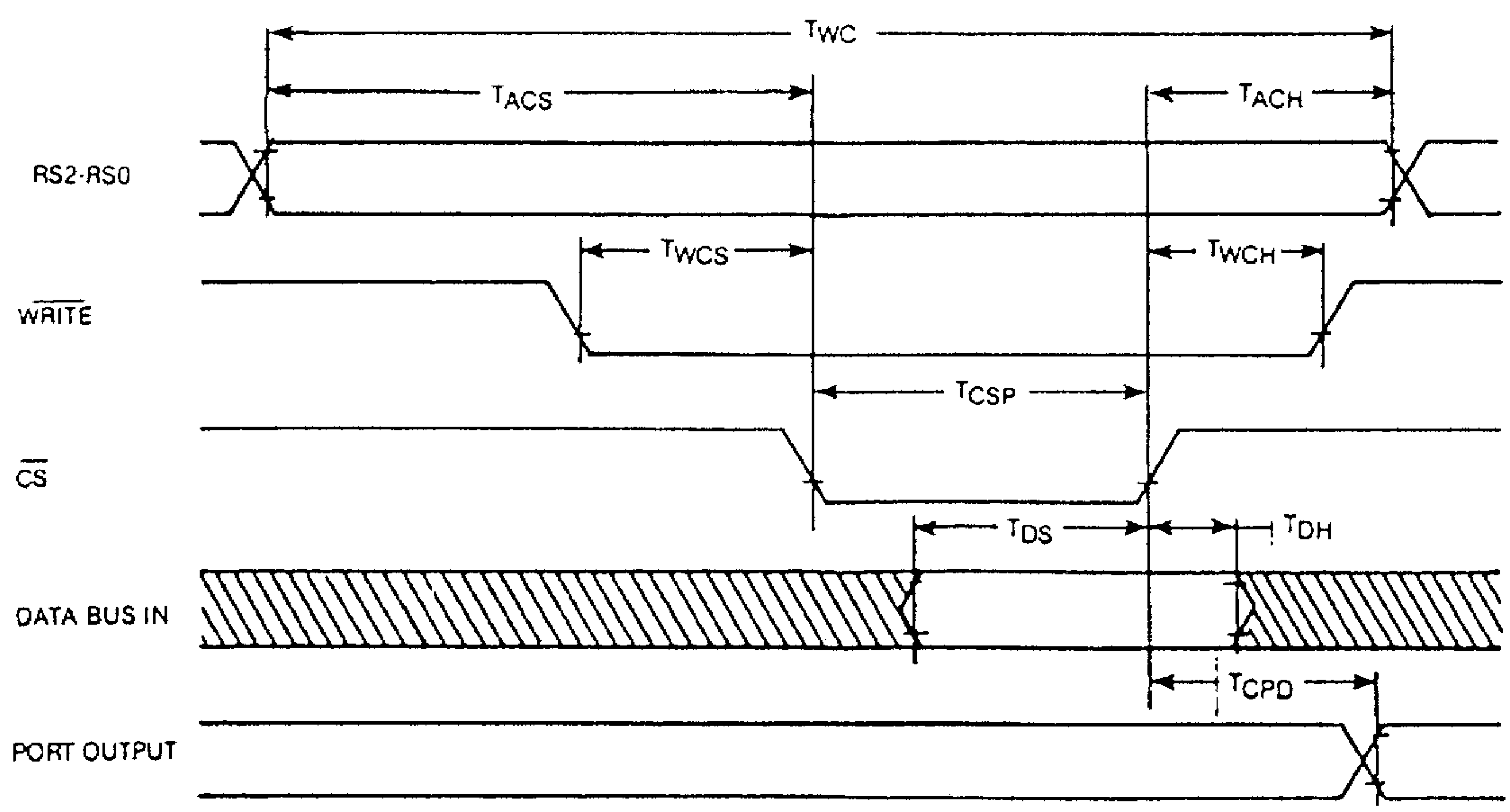
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	[illegible]
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	1.5	V_{CC}	[illegible]
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	1.2	+0.8	[illegible]
Input Leakage Current V_{in} = 0 to 5.0 V WRITE, RES, CS, RS2-RS0	I_{IN}	0	± 1.0	± 2.5	μA
Three-State (Off-State) Input Current (V_{in} = 0.4 to 2.4 V V_{CC} = max) D0-D7, PA0-P7, PB0-PB7, PC0-PC7	I_{TSI}	0	± 2.0	± 10	μA
Output High Voltage (V_{CC} = min, Load = 200 μA)	V_{OH}	2.4	3.5	V_{CC}	V
Output Low Voltage (V_{CC} = min, Load = 3.2 mA)	V_{OL}	V_{SS}	0.2	0.4	V
Output High Current (Sourcing) (V_{OH} = 2.4 V)	I_{OH}	−200	−1000	—	μA
Output Low Current (Sinking) (V_{OL} = 0.4 V)	I_{OL}	3.2	—	—	mA
Supply Current	I_{CC}	—	50	100	mA
Input Capacitance (V_{in} 0V, T_A = 25°C, f = 1.0 MHz) D0-D7, PA0-PA7, PB0-PB7, PC0-PC7 WRITE, RES, RS2-RS0, CS	C_{in}	—	7	10	pF
Output Capacitance (V_{in} = 0V, T_A = 25°C, f = 1.0 MHz)	C_{out}	—	7	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

READ CYCLE TIMING



WRITE CYCLE TIMING



Note: All timings referenced to V_{IL} max, V_{IH} min on inputs and V_{OL} max, V_{OH} min on outputs.

READ CYCLE TIMING

Symbol	Characteristic	6525 MIN	6525 MAX	6525A MIN	6525A MAX	6525B MIN	6525B MAX	UNITS
T_{RC}	Read Cycle	450	—	225	—	165	—	ns
T_{ACC}	Access Time[1]	—	450	—	225	—	155	ns
T_{CO}	$\overline{CS}$ to Output Valid	—	270	—	120	—	70	ns
T_{ACS}	RS to $\overline{CS}$ Set Up	0	—	0	—	0	—	ns
T_{ACH}	RS to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{RCS}	R/W high to CS Set Up	0	—	0	—	0	—	ns
T_{RCH}	R/W high to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{OTD}	$\overline{CS}$ to Output off Delay	20	120	20	120	20	100	ns
T_{PDS}	Port Input Set Up	120	—	60	—	40	—	ns
T_{PDH}	Port Input Hold	150	—	150	—	150	—	ns

NOTE 1 — Access time measured from later of R/W high or RS stable.

WRITE CYCLE TIMING

Symbol	Characteristic	6525 MIN	6525 MAX	6525A MIN	6525A MAX	6525B MIN	6525B MAX	UNITS
T_{WC}	Write Cycle	450	—	225	—	165	—	ns
T_{ACS}	RS to $\overline{CS}$ Set Up	0	—	0	—	0	—	ns
T_{ACH}	RS to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{WCS}	R/W low to $\overline{CS}$ Set Up	0	—	0	—	0	—	ns
T_{WCH}	R/W low to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{DS}	Data Bus to $\overline{CS}$ Set Up	150	—	100	—	50	—	ns
T_{DH}	Data Bus to $\overline{CS}$ Hold	0	—	0	—	0	—	ns
T_{CPD}	$\overline{CS}$ to Port Out Delay	—	1000	—	500	—	330	ns
T_{CSP}	$\overline{CS}$ Pulse Width	420	—	200	—	150	—	ns

6525 INTERNAL REGISTERS

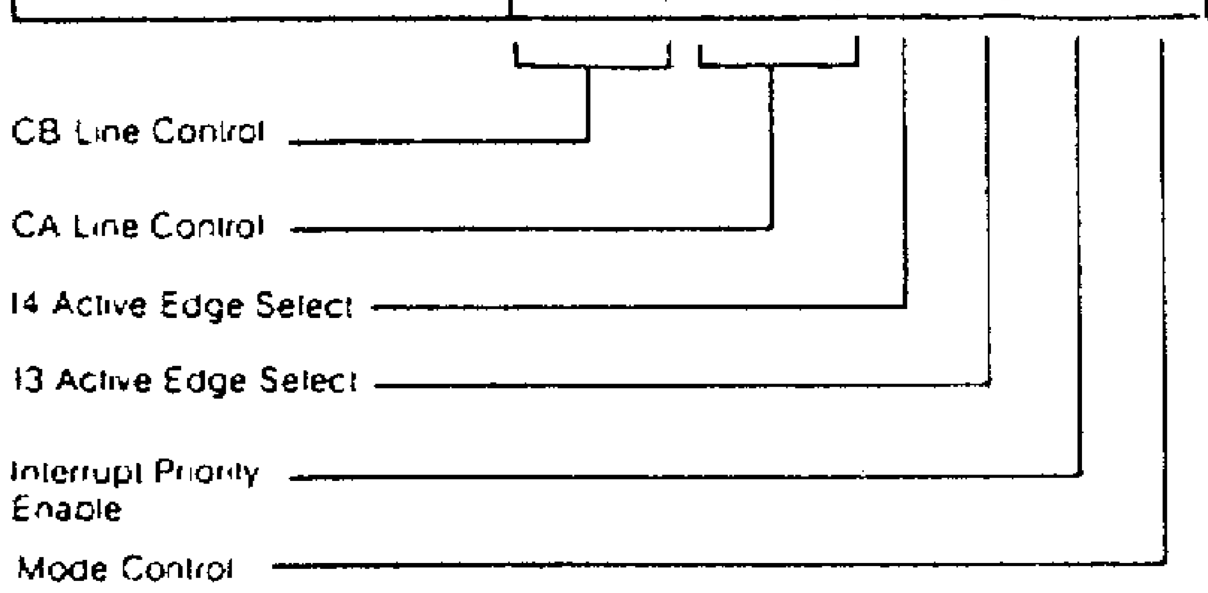
ADDRESS				REGISTER BITS								REGISTER NAME	COMMENT
RS2	RS1	RS0	MC	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	X	PA_7	PA_6	PA_5	PA_4	PA_3	PA_2	PA_1	PA_0	Port Register A (PRA)	
0	0	1	X	PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0	Port Register B (PRB)	
0	1	0	0	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	Port Register C (PRC)	
0	1	0	1	CB	CA	$\overline{IRQ}$	IL_4	IL_3	IL_2	IL_1	IL_0	Port Register C (PRC)	Handshake and Interrupt Latches (MODE 1)
0	1	1	X	DA_7	DA_6	DA_5	DA_4	DA_3	DA_2	DA_1	DA_0	Data Direction Register A (DDRA)	0=Input; 1=Output
1	0	0	X	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Data Direction Register B (DDRB)	0=Input; 1=Output
1	0	1	0	DC_7	DC_6	DC_5	DC_4	DC_3	DC_2	DC_1	DC_0	Data Direction Register C (DDRC)	0=Input; 1=Output (MODE 0)
1	0	1	1	—	—	—	M_4	M_3	M_2	M_1	M_0	Interrupt Mask Register	0=Mask, 1=Enable (MODE 1)
1	1	0	X	CB_1	CB_0	CA_1	CA_0	IE_4	IE_3	IP	MC	Control Register (CR)	Mode Selected by MC
1	1	1	1	—	—	—	AI_4	AI_3	AI_2	AI_1	AI_0	Active Interrupt Register (AIR)	

6525 FUNCTIONAL DESCRIPTION

Control Register (CR)

The bits of the control register select the various operating modes of the 6525. Although the exact function of each bit is explained throughout the functional description, the functions are summarized here for convenience.

CONTROL REGISTER BIT	7	6	5	4	3	2	1	0
FUNCTIONAL DESIGNATION	CB_1	CB_0	CA_1	CA_0	IE_4	IE_3	IP	MC



MODE 0 — (MC=0)

In Mode 0, three 8 bit bi-directional ports (A, B, C) are available on the 6525. Each port has two associated read/write registers:

Data Direction Registers (DDRA, DDRB, DDRC)

Each bit of the data direction registers controls the corresponding pin of the associated port as follows:

DDR bit	Direction of port pin
0	Input (Output driver disabled)
1	Output (Output driver enabled)

Port Registers (PRA, PRB, PRC)

Reading the Port Register returns the logic states of the associated port pins. The pin voltage levels must meet the V_{IH} and V_{IL} specification limits to ensure valid data. (Excessive loading of the output driver may cause the data read to differ from the expected output.) If the port pin is programmed as an output by the DDR, the output driver is set to the last data written to the corresponding PR bit.

MODE 1 — (MC=1)

In Mode 1, the 6525 provides 2 8-bit bi-directional ports (A and B) as in Mode 0. By writing MC=1, Port C is automatically converted to a 5 level priority interrupt controller with interrupt output ($\overline{IRQ}$) and a handshake control line for each port (CA and CB).

MODE 0 PIN NAMES	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
MODE 1 PIN NAMES	CB	CA	$\overline{IRQ}$	I4	I3	I2	I1	I0

Port Register C — PRC (Mode 1)

All bits of the PRC can be read as in Mode 0 but the state of the interrupt latches, rather than the interrupt pins, is returned in the five low order bits of PRC. Writing "0" to a PRC bit clears the corresponding interrupt latch but has no effect on the CA, CB, or $\overline{IRQ}$ outputs. Writing "1" to a PRC bit has no effect on Mode 1.

MODE 0 BIT NAMES	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
MODE 1 BIT NAMES	CB	CA	$\overline{IRQ}$	IL_4	IL_3	IL_2	IL_1	IL_0

CA and CB Outputs — (PC6 and PC7)

CA and CB may be used as general purpose outputs or as data transfer signals for ports A and B. The operation of CA and CB is selected as follows:

CA_1	CA_0	CA OUTPUT MODE	CB_1	CB_0	CB OUTPUT MODE
0	0	Set high by active transition of I3. Reset low by reading PRA	0	0	Set low by writing PRB. Reset high by active transition of I4.
0	1	Pulses low for at least 500 ns after reading PRA.	0	1	Pulses low for at least 500 ns after writing PRB.
1	0	CA low	1	0	CB low
1	1	CA high	1	1	CB high

$\overline{IRQ}$ Output — (PC5)

The Interrupt Request is set low when an unmasked interrupt (see below) is activated. $\overline{IRQ}$ is reset high by reading the Active Interrupt Register (AIR). The $\overline{IRQ}$ output has an open drain to allow wire AND tying of multiple outputs.

I4, I3, I2, I1, I0 Inputs — (PC4-PC0)

The five low order pins of Port C are interrupt inputs in Mode 1. A negative (high to low) transition on I2, I1 or I0 sets the corresponding latch in PRC to indicate an interrupt, while either transition of I3 or I4 can be selected to set its latch as follows:

IE3	I3 EDGE SELECTION	IE4	I4 EDGE SELECTION
0	I3 sets IL_3 latch on negative (hi—low) transition.	0	I4 sets IL_4 latch on negative transition.
1	I3 sets IL_3 latch as positive (low—hi) transition.	1	I4 sets IL_4 latch on positive transition.

Interrupt Mask Register (DDRC in Mode 1)

In Mode 1, the five low order bits of the DDRC are utilized as interrupt mask bits of the five corresponding interrupt latches. Writing a "1" to the mask register enables the corresponding interrupt latch to initiate an interrupt while a "0" masks the interrupt latch output. Masking does not prevent the interrupt latch from being set by an active input transition. The interrupt mask register can be read and written.

Active Interrupt Register (AIR)

The five low order bits of the AIR contain the present interrupt status of the 6525. A "1" in a bit of the AIR indicates that the corresponding interrupt is active. Reading the AIR clears all AIR bits and resets any interrupt latch which had set a bit in the AIR. READING AND WRITING OF THE AIR AFFECTS THE INTERRUPT PRIORITY STACK. Therefore, the AIR should be accessed only in strict accordance to the following rules:

1. READ THE AIR ONLY TO INDICATE BEGINNING OF INTERRUPT SERVICE.
2. WRITE THE AIR ONLY TO INDICATE CONCLUSION OF INTERRUPT SERVICE.

DESCRIPTION OF PRIORITY INTERRUPT OPERATION

No Priority Operation Selected — (IP=0)

When an active transition occurs on an interrupt input (see I4-I0), the corresponding interrupt latch is set. If this latch is not masked, the corresponding bit of the AIR is set, $\overline{IRQ}$ (PC5) is activated low, and other interrupt latches are prevented from setting new bits in the AIR. After reading the AIR, the interrupt latch corresponding with the bit set in the AIR is cleared to await new input and $\overline{IRQ}$ is reset high. Any interrupt latches remaining set will now restart this interrupt sequence. If multiple interrupts have been received in the interim, multiple bits will be set in the AIR and all corresponding interrupt latches will be cleared when the AIR is read. Therefore, software must recognize the occurrence of multiple interrupts when no priority operation is selected.

Priority Operation Selected — (IP=1)

The five interrupt inputs have a fixed priority: I4 > I3 > I2 > I1 > I0. When priority operation is selected, only the highest priority interrupt is placed in the AIR, ensuring only one bit set in the AIR at any time. When an interrupt occurs, the corresponding interrupt latch is set as before but is then compared with the present active interrupt, the new bit in the AIR is set and $\overline{IRQ}$ is activated low. When AIR is read, the contents of the AIR are pushed onto a level stack for comparison with subsequent interrupts and AIR is cleared.

After servicing the new interrupt, the processor must write to the AIR (clearing the AIR) to instruct the 6525 that this interrupt service is complete. The previous interrupt status is then recalled (popped) to the top of the stack to be used for evaluating new interrupt inputs. Interrupts of lesser priority than the active interrupt are masked until all higher level interrupts are acknowledged and completed by the processor (as indicated by AIR reads and writes). When all higher priority interrupts have been serviced, the 6525 will allow a lower priority interrupt to indicate a new interrupt sequence.

The following examples illustrate the priority interrupt operation:

A. Single Interrupt

1. Interrupt received by negative transition on I1.
2. Interrupt latch 1 (IL_1) is set.
3. Bit A_1 set in AIR.
4. $\overline{IRQ}$ activated low.
5. Processor responds by reading AIR to determine which interrupt occurred.
6. AIR is pushed onto interrupt stack and latch 1 is cleared.
7. AIR is cleared and $\overline{IRQ}$ reset high.
8. Upon completion of service, processor writes to AIR.
9. Interrupt stack is popped, restoring previous interrupt status.

B. Lower priority interrupt received during active interrupt
   1. I1 received and latched.
   2. A_1 is set and $\overline{IRQ}$ activated low.
   3. Processor reads AIR to determine I1 is active.
   4. AIR pushed onto stack and IL_1 cleared.
   5. AIR cleared and $\overline{IRQ}$ reset high.
   6. Processor is servicing I1 while I0 occurs and sets IL_0.
   7. Interrupt stack prevents lower priority IL_0 from initiating a new interrupt.
   8. Upon completion of I1 service, processor writes to AIR, popping I1 interrupt out of stack.
   9. IL_0 is now permitted to initiate a new interrupt service.

C. Higher priority interrupt received during active interrupt
   1. Interrupt I1 received and latched.
   2. A_1 is set and $\overline{IRQ}$ activated low.
   3. Processor reads AIR to determine I1 is active.
   4. AIR is pushed onto stack and IL_1 cleared.
   5. AIR cleared and $\overline{IRQ}$ reset high.
   6. Processor is servicing I1 when I2 occurs and sets IL_2.
   7. A_2 is set and $\overline{IRQ}$ activated low because IL_2 has higher priority than I1 in stack.
   8. Processor recognizes interrupt request and calls interrupt service routine.
   9. Processor reads AIR to determine I2 is active.
   10. New AIR is pushed onto interrupt stack and IL_2 cleared.
   11. AIR cleared and $\overline{IRQ}$ reset high.
   12. Processor services I2.
   13. Upon completion of I2 service, processor writes to AIR popping I2 interrupt from stack, restoring I1 status to top of stack (still preventing an I0 interrupt).
   14. Processor return from interrupt resumes services of suspended I1 routine.
   15. Upon completion of I1, processor writes to AIR, popping I1 interrupt from stack, leaving no active interrupts.

6525 INTERFACE AND CONTROL

Initialization

A low on the $\overline{RES}$ pin clears all 6525 internal registers. This puts the 6525 in Mode 0 with all three ports selected as inputs (floating), preventing any conflicts on the bi-directional port lines. For port pins to be used as outputs, the desired output data may be written to the port register before enabling the output driver. This sequence can eliminate undesired output conditions when the outputs are enabled via the DDR.

When selecting Mode 1, all interrupt inputs and IE3, IE4 must be stable before writing MC bit to "1." If this can not be ensured, the interrupt latches (PRC_4-PRC_0) should be cleared by writing 0 to PRC after MC=1 and before unmasking the interrupt latches. Similarly, if CA and CB are to be used as data transfer handshake lines, no PRA reads or PRB writes should occur after RES or before actual data transfers are to begin.

Processor Interface

The 6525 is a fully static device with interface characteristics similar to a static RAM. To read, the RS and R/W lines are stabilized and then $\overline{CS}$ is switched low, gating the desired register onto the system data bus. (In 650X systems, $\overline{CS}$ may be gated with Ø2). The system timing must accommodate both the T_{ACC} (address) and T_{CO} (chip select) delays before requiring valid data. To write to the 6525, similar timing is required, with the processor providing valid write data at least $_{DS}$ before $\overline{CS}$ switches high. To guarantee proper operation of the 6525, THE R/W LINE MUST BE STABLE ANY TIME $\overline{CS}$ IS LOW.